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CMP Solutions for the Integration of High-K Metal Gate Technologies

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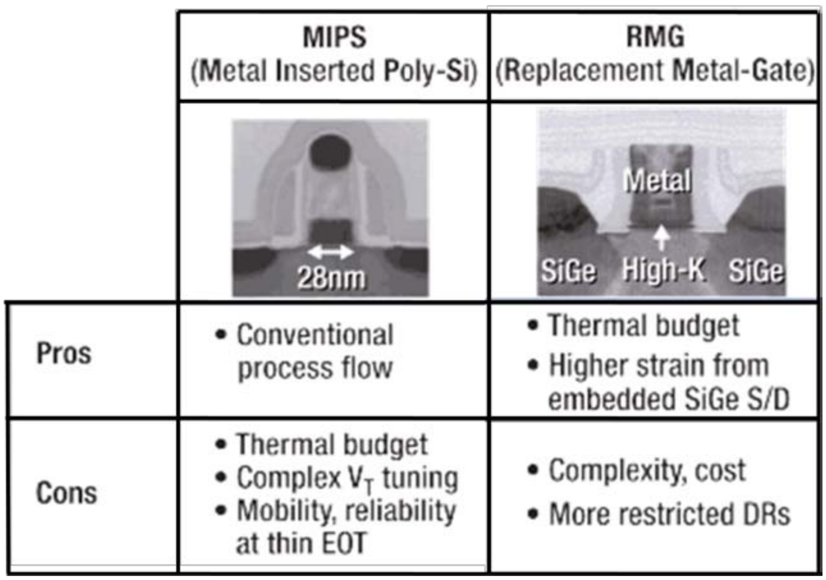
In order to enable high-k metal gate technology, new CMP steps and slurries are needed to meet the stringent planarity and defect requirements for device performance. This paper will describe several of these slurry technologies in detail, including poly-open-polish, Aluminum CMP, and improvements required in Tungsten polishing. The keys to these technologies are outlined and polishing performance given in detail. The critical mechanisms involved in the material polishing for each of these steps are also introduced. All of these new technologies are needed in order to build a successful high-k metal gate device for advanced node integration via a replacement gate build strategy.

Introduction

The unabated drive to continue Moore's law has dominated technology advancement in the semiconductor industry. For more than 40 years, scaling of transistor level devices has led to the successful shrinking of device structures and performance improvements. In order to continue this drive for advancement, however, new materials and integration schemes for the transistor level have recently been introduced. Two main paths to integrate high-k metal gates for continuous performance scaling are actively being developed by the industry. The so-called gate-first (Metal Inserted Poly-Si) and gate-last (Replacement Metal-Gate) approaches have both pros and cons, as summarized in Fig. 1, for realizing the final gate structure. For low power applications (which do not require aggressive EOT and ultra low V_T), gate-first is arguably the most appropriate choice. The benefits of the gate-last approach, in terms of extra strain and overall work function control, however, make gate-last the best option when both high-performance and low-power applications are required.

Intel Corporation's announcement of a replacement gate build strategy for high-k metal gate technology in their 45 nm device node has inspired designs for the sub-32 nm node (1). In order to enable this technology advancement, new CMP steps and slurries are needed to meet the stringent planarity and defect requirements for device performance. In this build process normal silicon dioxide growth is replaced by high-*k* gate dielectric formation. After normal dielectric deposition, a stop on polysilicon polish step exposes poly gates, and a gate trench is formed by removal of the dummy poly. Barrier metals and aluminum are deposited in the gate trench and then planarized using a metal polish step. Both gate-fill and subsequent process steps are extremely sensitive to the variation in topography resulting from both the poly-gate and metal-gate CMP processes (2). After completion of the aluminum polishing step, contact formation is completed using standard tungsten processing steps. For advanced node device build, the planarity and dielectric loss that can be achieved using SS-W2000 polishing does not satisfy the integration requirements. Improvements to this process step through both formulation and process improvements are needed to accomplish success device builds.



	MIPS (Metal Inserted Poly-Si)	RMG (Replacement Metal-Gate)
	28nm	Metal SiGe High-K SiGe
Pros	• Conventional process flow	• Thermal budget • Higher strain from embedded SiGe S/D
Cons	• Thermal budget • Complex V_T tuning • Mobility, reliability at thin EOT	• Complexity, cost • More restricted DRs

Figure 1. Pros and Cons of Two Primary High-k Metal Gate Build Strategies

The steps outlined above have presented consumable suppliers an opportunity to provide value through innovation of new products to meet new customer requirements involved in the replacement gate build process. This contribution will describe how new slurry technologies can address the needs of the industry, and enable the replacement metal-gate build. Technologies for poly-open-polish (POP), aluminum and tungsten bulk metal CMP, and various buff slurry technologies will be presented. The mechanisms governing these slurry technologies are also introduced and the challenges that remain are addressed.

Results

Poly-Open-Polish (POP

As integration schemes have advanced, there has been an ongoing need to develop slurries and methods capable of removing silicon nitride layers at relatively high rates of removal. These so called “Nitride” slurries can have a variety of requirements regarding the selectivity to other films and the ultimate removal rates. The most common steps require a high silicon nitride removal rate with tunable selectivity to silicon dioxide. From an application standpoint, nitride slurries are thought to be used in double patterning technology, advanced transistor build (e.g. FinFet) and ‘poly open polish’ (POP) for high-k metal gates (Fig.2). Along with these requirements, RMG also calls for low or ‘stop on polysilicon’ removal rates in addition to high nitride removal rates and tunable oxide removal. This process is used to remove the nitride layer cap above a formed gate structure that contains a polysilicon working metal. The polysilicon gate is subsequently removed by etching, and then backfilled with aluminum metal.

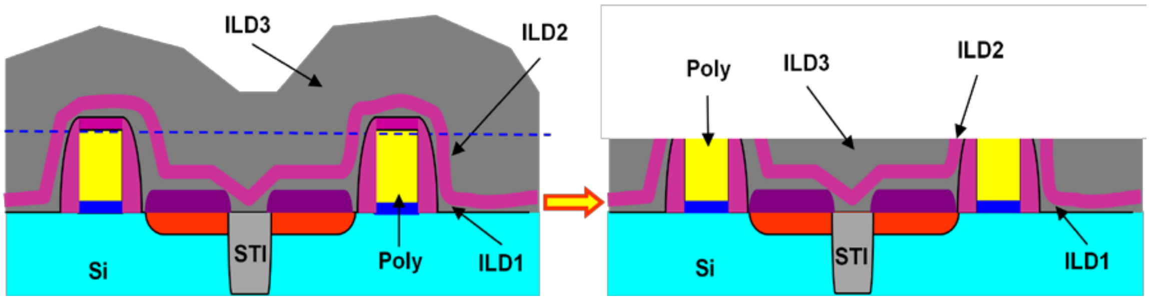


Figure 2. First CMP step clearing bulk oxide and stop on nitride. Second step nitride/oxide polish stopping on poly.

Due to the stringent cost and defect requirements necessitated by this integration step, our initial studies focused on the use of colloidal silica abrasives for this application. In order to achieve selective polishing to silicon dioxide, it was found that acidic pH was preferred using this strategy. This follows from the proposed mechanism of silicon nitride removal during polishing (3).

$$Si_3N + H_2O \longrightarrow Si_2NH + Si\text{-}OH \quad [1]$$
$$Si_2NH + H_2O \longrightarrow SiNH_2 + Si\text{-}OH \quad [2]$$
$$SiNH_2 + H_2O \longrightarrow Si\text{-}OH + NH_3\uparrow \quad [3]$$

Nitride polish rates are dependent on the kinetics of the hydrolysis of the nitride film, which is pH dependent. Pad choice and polish conditions also play key roles. Data presented here are based on two different colloidal silica platforms. Initial nitride slurry development, involved the use of a 50 nm colloidal silica particle, in which specific nitride rate promotion additives were also added (N1113). Promotion additives are based on various organic acids (4). Figures 3 and 4 show the dependence of nitride and oxide removal rates on the concentration of a specific phosphonic acid. The data shows that the overall nitride selectivity can be tuned with abrasive and additive concentrations. A detailed mechanism as to how this additive promotes nitride removal remains elusive. It is believed, however, that this chemical plays multiple roles including enhancing the rate-limiting hydrolysis step and modulating abrasive/surface (pad/wafer) interactions. The anionic nature of the additive may act as a bridge between the cationic particles and cationic nitride surface, reducing electrostatic repulsion, thus lowering the energy barrier for particle-film contact. While this slurry system provides the necessary nitride to oxide performance, achieving low polysilicon removal rates for RMG has remained challenging.

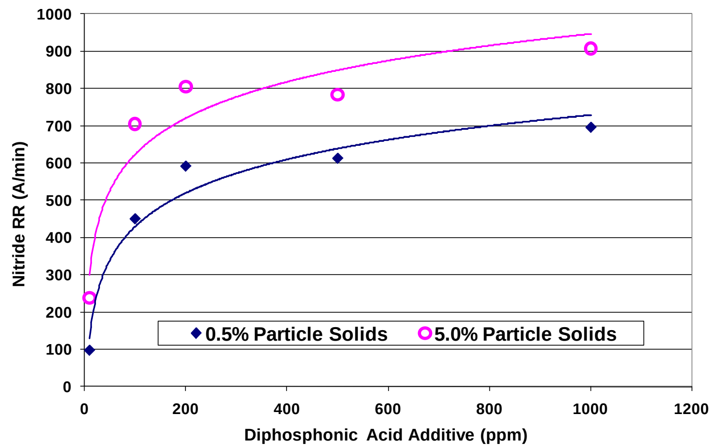


Figure 3. Nitride RR vs N1113 slurry additive level

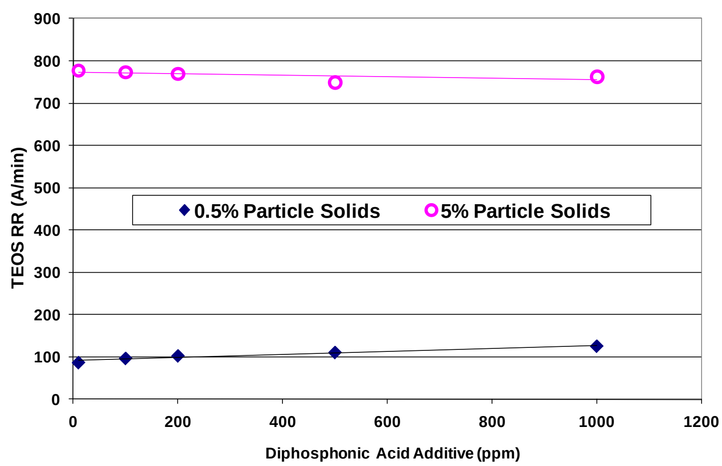


Figure 4. TEOS RR vs N1113 slurry additive level

To address this performance gap, another nitride slurry platform (N310x), utilizes uniquely modified colloidal silica. In this system, the particle is modified such that the normally cationic colloidal silica becomes highly negative (even at strongly acidic pH). This eliminates the necessity for addition of nitride promotion chemistry. In order to achieve the performance desired for RMG build, additives to selectively suppress the removal of polysilicon are incorporated in the slurry. Figure 5 shows blanket polish results on two different pad types for the different slurry platforms.

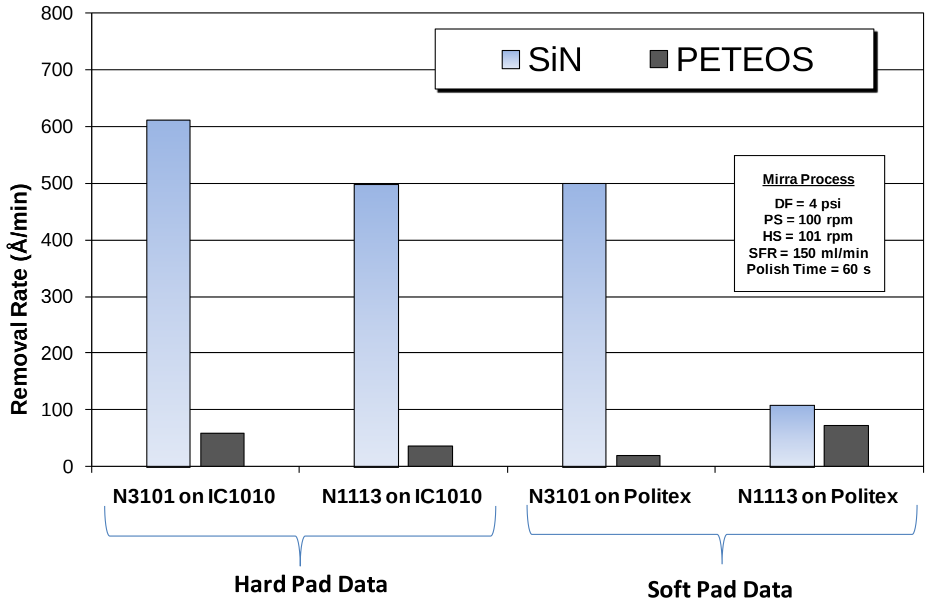


Figure 5. N1113 and N3101 polish data on hard and soft pads

The data show that while both slurries are selective to oxide, N3101 shows greater overall nitride rates on both pads and excellent performance and selectivity on the soft Politex pad. This performance distinction is important given the inherently better defectivity performance of the soft pad, which is desirable for this sensitive FEOL application. The unique particle employed in N31XX shows a naturally low oxide removal rate due to charge repulsion with the anionic oxide film. Conversely, the anionic particle is attracted to the cationic nitride surface, and is more nucleophilic in regards to particle surface reactions, promoting removal of material.

For POP, it is important to be able to selectively suppress the polysilicon removal relative to the other dielectric films present. In addition, due to unique customer requirements, the ability to modulate silicon dioxide removal is desired. While these requirements have proved challenging, they have recently been accomplished in the N310x platform. Certain organic based additives have demonstrated the ability to selectively suppress the polysilicon rate relative to nitride and oxide. By decreasing the pH of the slurry, the oxide rate can be independently increased, (Fig. 6). By employing both of these technologies, our N3107 slurry has the required performance for POP relative to other slurries introduced thus far. By decreasing the pH in N3107 the TEOS removal rate can be selectivity tuned relative to the other films for integration schemes requiring some removal of that material (N3108, Fig. 6).

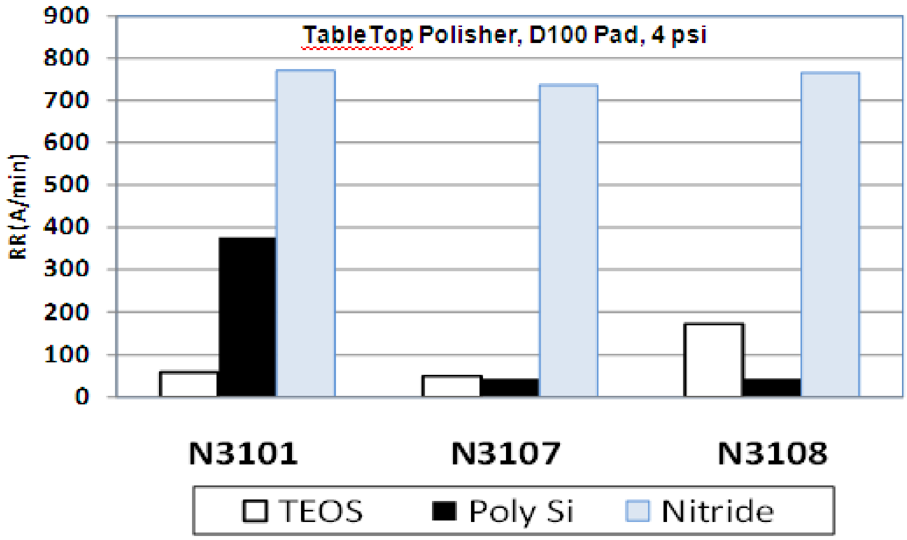


Figure 6. Comparison of silicon nitride, silicon dioxide and polysilicon removal in the N310X polishing series (2% abrasive)

In summary, it has been shown that new colloidal silica based slurries have been developed to give moderate nitride, and tunable oxide and polysilicon removal rates. Performance is achieved through the intimate knowledge of abrasive characteristics combined with the discovery of specific classes of rate control additives to selectively tune performance on various film materials. While these slurries meet the initial requirements of POP for RMG, additional systems based on ceria abrasives are under investigation for further performance benefits.

Aluminum CMP

While prevalent in BEOL processing, aluminum metal is typically removed via reactive ion etch processes. For RMG build, however, the planarity and defect requirements necessitate the employment of a CMP process. While we have been working on CMP processes for aluminum planarization for some time, only recently has this scheme been adopted in production. Our Novus^{tm}A7000 series of products has been designed to meet the stringent requirements needed for metal CMP to build a successful metal gate. Figure 7 shows a simplified view of the roles of various slurry components on the overall removal mechanism in this series of products. In this slurry system, both small organic molecules (C, Fig. 7) and polymers (PX, Fig 7) are employed to obtain the desired film which controls both removal and final dishing. Critical to obtaining acceptable film removal while limiting unwanted defect performance, is balancing the complexation/dissolution kinetics while minimizing unwanted removal of underlying metal.

Table 1. Electrochemical parameters for representative A7100 series slurry

	V_{diss}, V MSE	**I_{diss}, Å/min**	**ΔV w/ abrasion**	**AF w/ abrasion**	**V_{corr}, V MSE**	**I_{corr}, Å/min**	**ΔV w/o abrasion**	**AF w/o abrasion**
Al	-1.545	288	250	2.7	-0.718	2	140	10
Ti	-1.295	306			-0.578	2		

If the mechanism of Al polishing involved the continuous formation and removal of its oxide, as suggested by Kaufman et. al. for W polishing, or a competition between the passivation rate and oxide removal, as suggested in early work by Wang et. al., the overall polishing rate would be equal to the electrochemical rate (5,6). The measured I_{diss} electrochemical removal rate of aluminum (at 3 psi) in this work is barely higher than 300Å/min (Table 1) while the overall polishing rate at the same DF is more than 10 times higher. Moreover, the polishing rate shows Prestonian behavior (Fig. 8), underlying the importance of the mechanical process for the overall aluminum removal. Prestonian behavior for Al CMP has been reported in the literature, but often as a complex process, where the linearity of the polishing rate with variation of the pressure and the velocity follow two different slopes (7). A similar mechanism invoking removal of underlying metal was suggested for the CMP of aluminum in phosphoric acid (8). This mechanism proposes that polishing particles cut through the surface film and remove small amounts of non-oxidized metal. Removal of non-oxidized metal cannot be determined by electrochemical tests, as they only measure the current caused by the metal oxidation process. In the case of aluminum, such a mechanism is readily noticeable, in many instances (e.g. in electrochemical tests), by the formation and accumulation of so called “black debris”, i.e. small metallic particles, surrounded by a fast forming oxide. It is worth noting that in our polish testing this black debris was not observed. This does not necessarily suggest that aluminum is not removed in its un-reacted state, but does indicate that the metallic particles are most likely very small, readily and fully oxidized and removed from the pad with fast kinetics.

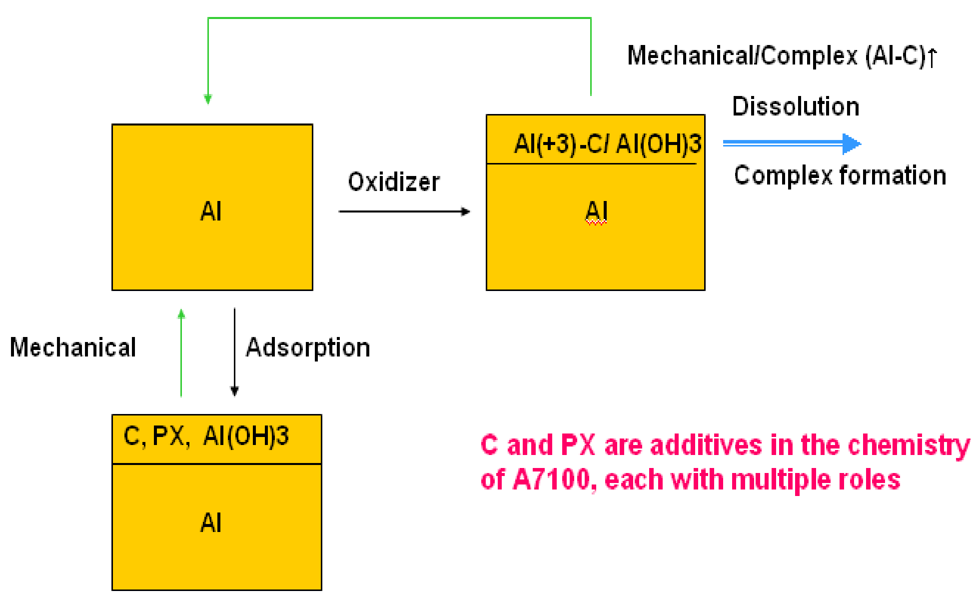


Figure 7. Simplified mechanism of polishing of aluminum in Novus™ series of products

In spite of the overwhelming effects of mechanical action, chemistry still plays a crucial role in the overall process: it is responsible for the type of the surface film formed, which in turn affects the initiation of mechanical surface removal and controls recess, dishing, erosion, and corrosion.

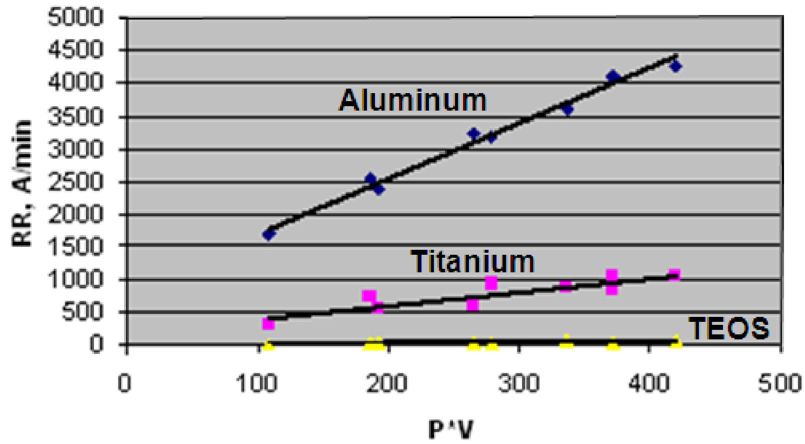
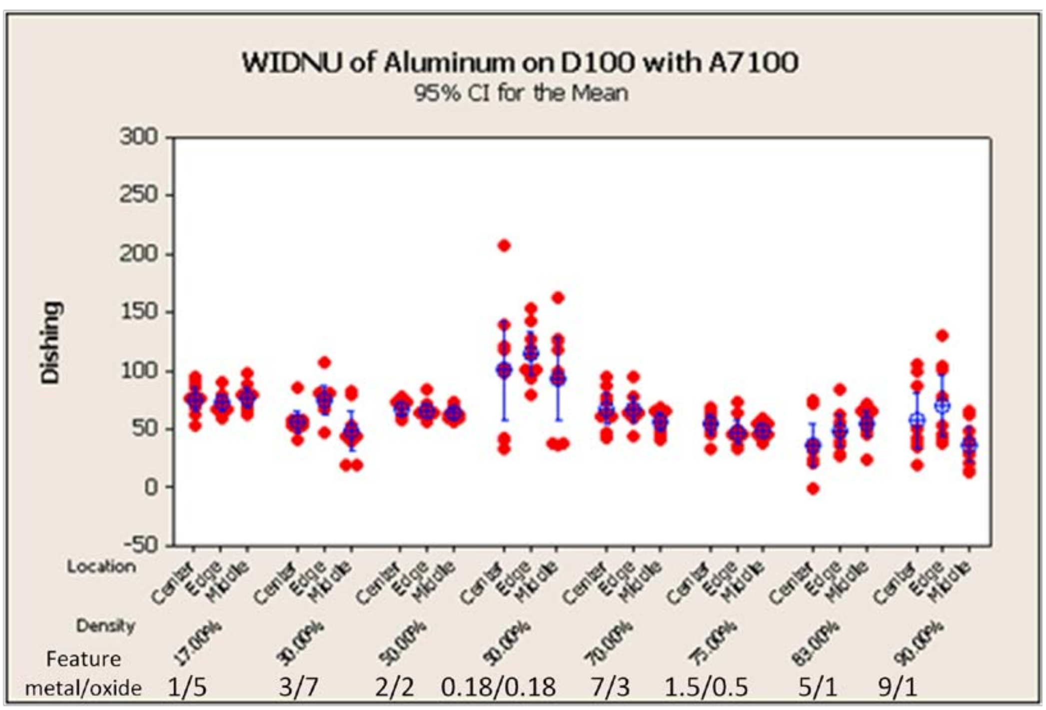


Figure 8. Polishing of aluminum in representative A71XX slurry

In addition to slurry considerations, process and pad choices play a critical role in achieving the extremely low topography requirements needed for RMG aluminum CMP. Figure 9 shows the difference in dishing non-uniformity between IC1000 and Epic™ D100 polishing pads using the A7100 polishing slurry.



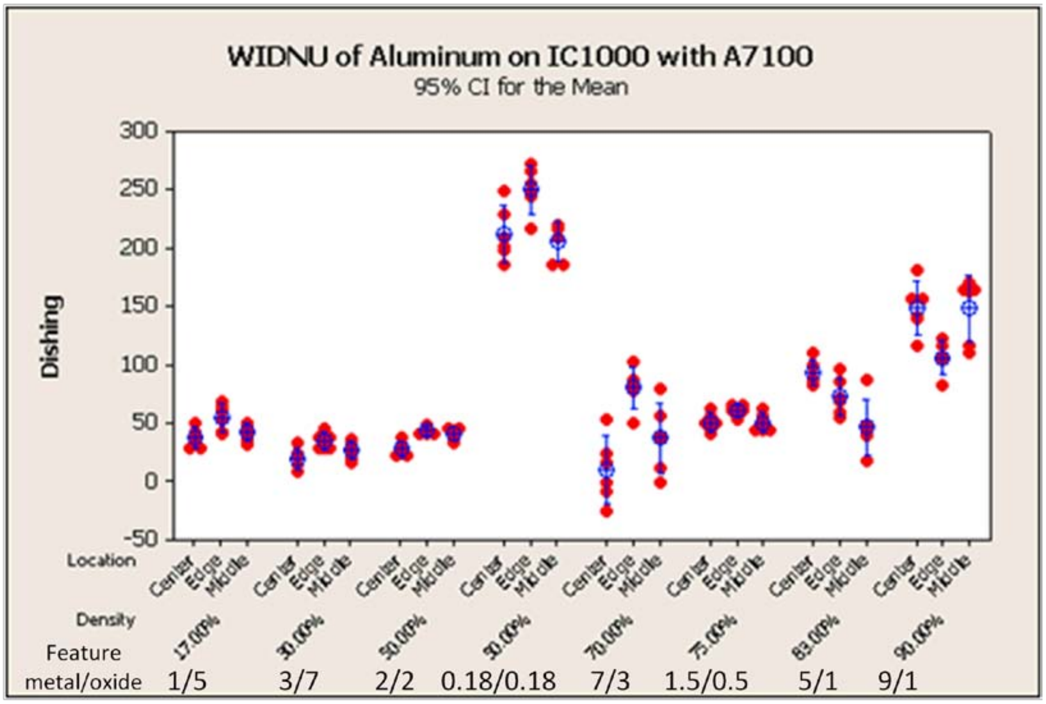


Figure 9. Comparison of feature dependent dishing between D100 and IC1000 pad with A7100 polishing slurry

Customer targets of near zero dishing can be approached on either pad. The D100 pad, however, shows less feature dependence on the dishing performance, which is advantageous to customers implementing RMG (it should be noted that the 0.18x0.18 micron feature is susceptible to deposition defects which may drive a statistically higher dishing value for that particular site). In summary, both slurry chemistry and process parameters must be taken into consideration in order to achieve the extremely challenging topography and defect requirements needed for high-k metal gate integration via a gate-last process incorporating aluminum CMP.

<u>Tungsten CMP</u>

Following gate formation, etch, and metal deposition, tungsten CMP must be performed. Figure 10 shows a TEM picture of both the PMOS and NMOS transistors after tungsten CMP (9). It can be seen that the desired structure contains a tungsten contact that is above the metal gate. In order to achieve this topography, both dielectric loss, and total topography must be controlled in the tungsten bulk step such that buffing can render the final, desired structure.

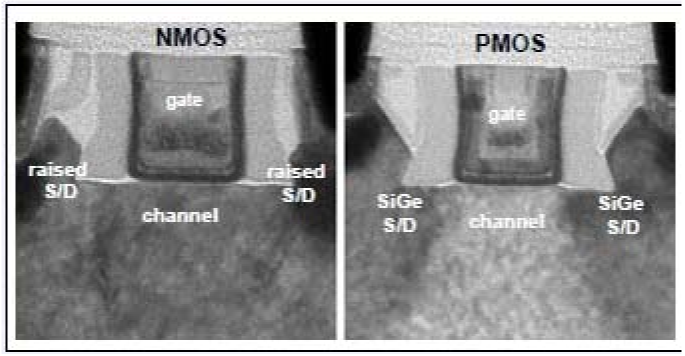


Figure 10. Intel's 32 nm NMOS and PMOS transistor structures

While thinner tungsten overburden can lead to lower removal rate requirements for this process step, tighter oxide budgets and topography requirements can greatly reduce the overpolish window. As shown in Fig. 11, current tungsten bulk slurries show increasing erosion as a function of oxide loss (overpolish time). While some overpolish is needed to compensate for non-uniform removal, this effect can lead to varying topography across the wafer surface and render the tungsten contacts far below the metal gate height. In addition, these current bulk tungsten slurries remove an excess of dielectric material to reach the topography target. In particular, while WIN tm W7300-B21 comes the closest to meeting customer topography requirements, it achieves this through its non-selective nature at the expense of dielectric loss.

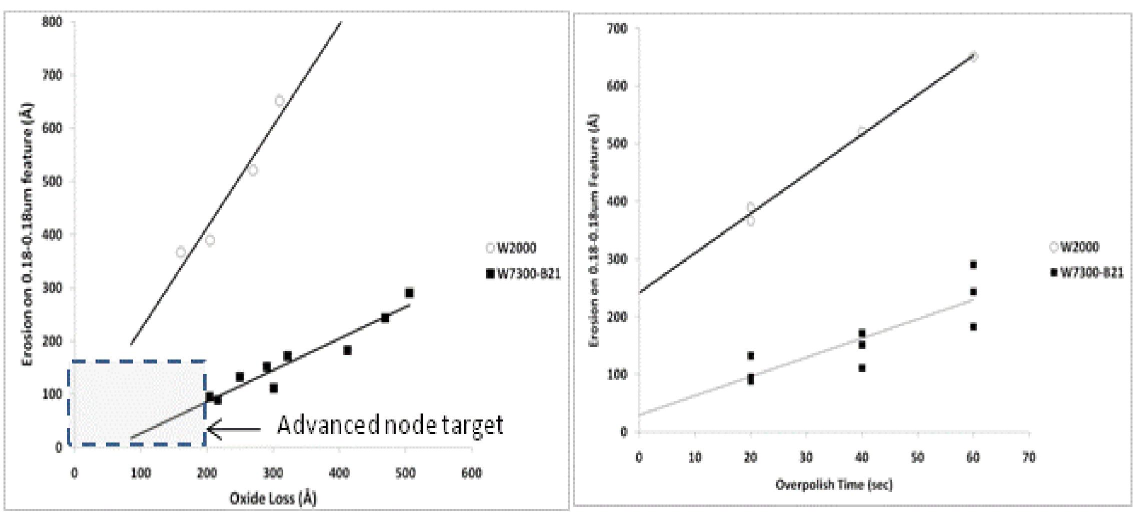


Figure 11. Topography vs Loss and Time for SS-W2000 and WIN tm W7300-B21

In addition to simple erosion and recess, edge-over-erosion (EOE) can be an issue in many metal polish slurries.   As shown in Fig. 12, EOE is an area of increased erosion at the outer edge of an array structure. Previous studies have shown that EOE is a mechanical process heavily influenced by the nature of the slurry abrasive particles and process conditions (10). In general, fumed silica particles give larger EOE than colloidal particles.

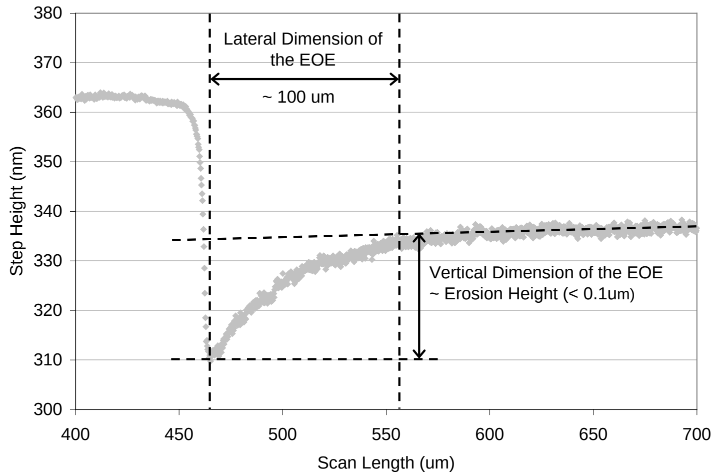


Figure 12. EOE in typical tungsten polishing

By minimizing EOE and achieving low topography, WIN tm W7300-B21 has proven to be a useful slurry for current technology nodes where dielectric loss is tolerated. Its low selectivity, improved chemistry, and colloidal abrasives lead to minimal EOE and low erosion with wider overpolish window, compared to SS-W2000. For RMG integration, however, the oxide loss this slurry produces exceeds customer's targets. The challenge, therefore, is in designing a slurry with the advantages of the colloidal based technology while minimizing dielectric loss. This can be achieved through optimization of abrasive properties, minimizing solids content, and improved tungsten rate control chemistry.

In order to address the needs of RMG, the move to an abrasive that contains the advantages of WINtm W7300-B21 with a surface charge similar to fumed silica was needed. This, along with the optimized chemistry of WIN tm W7573 allows for dilution to lower solids with only minor loss of tungsten removal rates which meets customer throughput requirements. As shown in Fig. 13, these diluted versions of W7573 can achieve low erosion (with no EOE) while decreasing the oxide loss within the requirements for RMG. Optimization/tuning of the chemistry in this system is leading to further improvements towards customer targets.

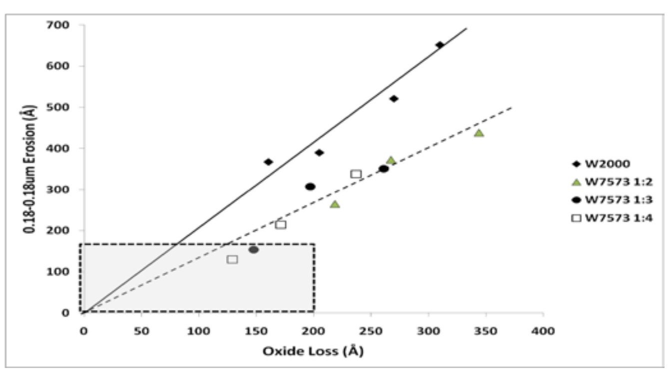


Figure 13. Oxide loss vs erosion for W7573 as function of dilution

In addition to low erosion, improvements in recess performance are also required in order to achieve tungsten contact protrusion requirements. Recess is largely driven by abrasive properties and the tungsten etch rate of a particular slurry. Tungsten etch rate is affected by both the etch inhibitor chemistry and the oxidizer content of the slurry. Improvements in the inhibition chemistry of the CMP slurry can help limit recess but, if improperly applied, can also have adverse effects on tungsten removal rates. Improvements in the slurry chemistry to increase tungsten removal rates can allow for reduced oxidizer needs, further reducing etch rate, as demonstrated in Fig. 14.

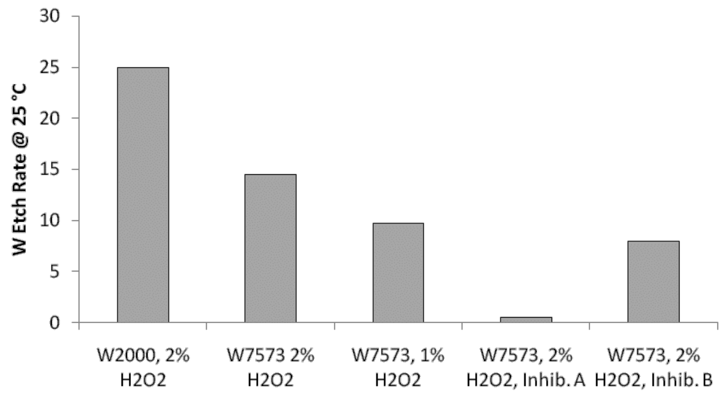


Figure 14. Tungsten etch rate vs. slurry for bulk polish slurries with varying oxidizer content and inhibitor type

In addition to changing bulk tungsten slurry performance, new requirements are present for buff CMP post metal clearing. The presence of the gate metal necessitates "stop-on-aluminum" performance for tungsten buffing. In order to achieve acceptable defectivity performance, this must also be achieved on a soft pad. Reformulation of WIN ^{tm} W7300-A18 with the addition of aluminum rate modifiers can achieve the desired results.

Summary

The development of RMG integration for the implementation of high-k metal gate technology has spurred the development of a variety of new CMP slurries. New technologies that can achieve aggressive topography and defectivity targets have been developed for all steps required for this build. Poly-open-polish and aluminum CMP are new technologies for the industry. Improvements beyond what is available in the marketplace today for tungsten CMP are needed to create advanced structures. Integration of these technologies is complex, and sensitivities to pad and process choice play a large role in achieving the desired performance metrics. Future development will focus on improvement of these slurry technologies in order to ease the implementation of CMP as a critical process step while design rules become tighter with technology advancement. This is another clear example of innovation in polishing capability enabling the commercialization of new device architectures.

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